## **REMARKS/ARGUMENTS**

Favorable reconsideration of this application is respectfully requested.

The specification is amended by the present response to correct minor informalities.

The changes made to the specification are deemed to be self-evident from the original disclosure, and thus are not deemed to raise any issues of new matter.

Applicants also note an Information Disclosure Statement (IDS) was filed in the present application on October 25, 2004. At this time applicants have not received confirmation of consideration of the references cited in that IDS. For convenience a copy of the IDS is submitted herein. Applicants request a return of the provided form PTO-1449 initialed by the Examiner indicating the Examiner's consideration of the noted references.

Claims 1-24 are pending in this application. Claims 2, 3, 5, 6, 8, 9, 11, 12, 14, 15, 17, 18, 20, 21, 23, and 24 stand withdrawn from consideration as directed to non-elect inventions. Claims 1, 10, and 13 were rejected under 35 U.S.C. § 103(a) over U.S. patent 5,734,605 to Zhu et al. (herein "Zhu"). Claims 4 and 7 were rejected under 35 U.S.C. § 103(as) as unpatentable over Zhu in view of U.S. patent 6,111,781 to Naji. Claims 16, 19, and 22 were rejected under 35 U.S.C. § 103(a) as unpatentable over Zhu in view of U.S. Patent Application Publication 2002/01859196 A1 to Shin et al. (herein "Shin").

Addressing the above-noted rejections based on <u>Zhu</u>, and further in view of <u>Naji</u> or <u>Shin</u>, those rejections are traversed by the present response.

Initially, applicants note independent claim 1 is amended by the present response to clarify features recited therein. Specifically, independent claim 1 now additionally recites:

wherein data is written to the plurality of memory cells by making a write electric current flow to the plurality of bit lines of the first or second bit line group, writing data being determined by a direction of the

<sup>&</sup>lt;sup>1</sup> Applicants note this statement of the outstanding rejection does not indicate the rejection based on the combination of teachings of <u>Zhu</u> in view of <u>Naji</u>, but the basis for the rejection appears to rely on the teachings of <u>Naji</u>. Clarification of this rejection is respectfully requested.

write current flowing to the plurality of bit lines of the first or second bit line group.

The above-noted features are believed to be fully supported by the original specification for example at page 14, lines 2-6, and page 16, lines 5-8.

According to features now recited in claim 1, data is written to a plurality of memory cells by making a write electric current flow to the plurality of bit lines of the first or second bit line group. That is, such an operation is a multi-bit operation. Such a feature is noted in the original specification for example at page 14, lines 2-6.

Zhu is directed to a multi-layer magnetic tunneling junction memory cell. Zhu does not disclose or suggest such a multi-bit operation.

Moreover, amended independent claim 1 now additionally recites the writing data is determined by the direction of the write electric current flowing to the plurality of bit lines to the first or second bit line group. Such a feature is noted in the original specification for example at page 16, lines 5-8.

Zhu fails to teach or suggest the above-noted feature.

Further, <u>Naji</u> does not disclose either of the above-noted features, and thus <u>Naji</u> cannot overcome the deficiencies of <u>Zhu</u>.

More particularly, in <u>Naji</u> writing data is determined by a direction of a write electric current flowing to a digit line, and *not to a bit line*. In that respect, applicants draw attention to <u>Naji</u> at column 4, lines 17-22. The noted "digit line" in <u>Naji</u> corresponds to the write word line WWL in the present application, and the digit current of <u>Naji</u> corresponds to the write electric current in the present application.

In such ways, Naji does not disclose or suggest writing data being determined by a direction of a write electric current flowing to a plurality of bit lines of the first or second bit line group.

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In view of these foregoing comments, no combination of teachings of <u>Zhu</u> in view of Naji meets the limitations of amended independent claim 1, and the claims dependent

therefrom.

Moreover, no teachings in the further cited art to Shin can overcome the above-noted

deficiencies of Zhu in view of Naji.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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